REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application. Claims 1 and 4-7 are currently pending in this application. Claims 2-3 have been cancelled. No new matter has been added by way of the present amendment. For instance, the amendment to claim 1 is supported by previously presented claims 2-3, now cancelled. New claim 6 is supported by previously presented claims 1-3 as well as the Specification as originally filed at, for example, pages 7-8, paragraphs [0015]-[0016]. New claim 7 is supported by previously presented claim 1. Accordingly, no new matter has been added.

In view of the amendments and remarks herein, Applicants respectfully request that the Examiner withdraw all outstanding rejections and allow the currently pending claims.

Issues under 35 U.S.C. 102

Claims 1-5 stand rejected as being anticipated by USP 5,647,917 to Oida et al. (hereinafter "Oida"). Additionally, claims 1-5 stand rejected as being anticipated by USP 5,434,100 to Nakamura et al. (hereinafter "Nakamura"). Applicants respectfully traverse the outstanding rejections.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of anticipation. To establish a *prima facie* case of anticipation, the reference must teach each and every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993). "Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a

prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed. Circ. 1999) (quoting Titanium Metals Corp. v. Banner, 778 F.2d 775, 781 (Fed. Cir. 1985)).

The Examiner appears to believe that, since both Oida and Nakamura disclose epitaxial InP substrates having mirror finishes and a certain amount of dislocations, the substrates of both references would have less than 2 ppm haze. Applicants respectfully disagree.

The present invention is directed, *inter alia*, to an InP substrate for epitaxial growth, wherein the haze is not more than 1 ppm all over an effectively used area of the InP substrate, and an off-angle with respect to a plane direction is 0.05 to 0.10° (see, e.g. claim 1). According to the above configuration, both conditions of "the haze is not more than 1 ppm" and "an off-angle is 0.05 to 0.10°" are simultaneously satisfied. Thus, the presently claimed invention results in an epitaxial layer having unexpectedly superior surface morphology (see also claim 6).

Specifically, when epitaxial growth is carried out using the presently claimed substrate, the haze in the surface of the grown epitaxial layer can be controlled to a certain desired level of for example, not more than 1 ppm (see, e.g., claims 1 and 6). Accordingly, the substrate according to the present invention can be applied to semiconductor devices required to be highly integrated and sophisticated (see paragraphs [0016] and [0020] of the Specification).

In contrast, Oida and Nakamura merely disclose performing mirror polishing on a wafer having a certain dislocation. Both of the references are silent with regard to prevention of haze generation. As is known by those skilled in the art, haze is likely to be generated to some extent even when advanced mirror polishing techniques are applied. Further, it is particularly difficult to make the haze of an InP wafer be approximately 0. Therefore, one skilled in the art would not

arrive at the present invention, wherein a wafer having haze of not more than 1 ppm is used for epitaxial growth, based on the teachings of the prior art.

As previously noted, those of ordinary skill in the art recognize that the generation of haze is primarily caused by two reasons: (i) the quality of the crystal which is to be the substrate (determined, for example, by the dislocation); and (ii) the quality of the finishing processing of the substrate (determined, for example, by the mirror polishing). Notably, unless both qualities satisfy certain levels, the presently claimed condition of a haze of "not more than 1 ppm" cannot be achieved. Moreover, in a state where the dislocation level is extremely low, the generation of haze is likely to be influenced by the failure caused while the finishing processing is in progress. Haze can be generated even in a dislocation-free state (see, for example, JP2002-25954A [0018]-[0019], JP2001144056A [0005], JP2000-49123A [0004], JP08-31779A [0002]).

Applicants note that the above-cited references disclose GaAs wafers which are "haze free" or have haze levels of 0.1 ppm (see for example, JP0831779A [0011], and Table 1 in JP2002-25954A). However, the teachings of these references are directed to GaAs wafers, and not InP wafers. Applicants note that performing finishing processing on an InP wafer is much more difficult than doing so on a GaAs wafer. Thus, even if the polishing techniques for GaAs wafers disclosed in these references were applied on an InP wafer, it would not be possible to arrive at a haze level of "not more than 1 ppm", as presently claimed (see also the description in JP2004207417, paragraphs [0013] and [0014], where it is disclosed that GaAs and InP are considerably different in their properties and that the polishing method suitable for a GaAs wafer is not necessarily applicable to an InP wafer).

In the Advisory Action of July 16, 2009, the Examiner argued that the present Specification "fails to describe the polishing process of this application." The Examiner further argued that "if the polishing process...is new and unusual, then admits failing to meet the requirements of...112, first paragraph...Alternatively, the 112(1) requirement...might be met only by the 'usual method' of this application being an old and conventional prior art of polishing known at least as of 2000." Applicants respectfully disagree.

The present application discloses a novel combination of a substrate's haze level and off-angle, such that haze in an epitaxial layer is considerably enhanced even while possibly sacrificing the yield rate (which could also affect the cost of the manufactured product to some degree) (see paragraph [0025], wherein a haze of 0.5 to 0.8 ppm is disclosed). This claimed combination of haze level and off-angle has been discovered by Applicants for the first time. The claimed invention could not be obtained by merely experimenting with wafers subjected to conventional polishing processing.

Applicants note that, during semiconductor wafer manufacturing, decisions are made on a case-by-case basis as to whether to sacrifice yield rate to improve some other condition, such as haze level, etc. The required wafer specifications are determined according to the quality and function of the device to be manufactured therefrom. Thus, a wafer with certain specifications may be used in one application, but may not be used in another. In view of these circumstances, Applicants submit that the present Specification discloses the manufacturing steps and techniques required for a wafer to be used in highly integrated and advanced devices.

The skilled artisan is aware that manufacturing an InP wafer for epitaxial growth such that the haze in the surface after growth is within a certain desirable level (such as 1 ppm or less)

is extremely difficult, and that such level is hardly achieved at a large scale by merely improving or modifying the specifications of an individual wafer selected from among a massive number of wafers which are subjected to production at the same time. The present inventors have achieved the present invention by focusing on the microroughness in the surface of the epitaxial layer (a novel course of action; see [0009]).

Applicants respectfully submit that none of the cited references disclose or suggest the claimed combination of the haze and the off-angle of the substrate before epitaxial growth, and thus fail to anticipate the present invention.

In view of the above, reconsideration and withdrawal of this rejection are respectfully requested.

Issues under 35 U.S.C. 103(a)

Claims 1-5 stand rejected as being obvious over Oida and Nakamura in view of US Patent Publication 2004/0214407 to Westhoff et al. (hereinafter "Westhoff"), USP 4,846,927 to Takahashi (hereinafter "Takahashi"), USP 7,304,310 to Shortt et al. (hereinafter "Shortt") and "Born and Wolf" (hereinafter "Born"). Applicants respectfully traverse.

The remarks above in the context of the discussion of the rejections under 35 U.S.C. 102, are likewise applicable to the outstanding rejection. Additionally, Applicants respectfully submit that none of Westhoff, Takahashi, Shortt, or Born serves to cure the noted deficiencies of Oida and Nakamura.

Accordingly, Applicants respectfully submit that the present invention is not rendered obvious by the proposed combination of cited prior art references. Reconsideration and withdrawal of this rejection are thus respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and objections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Vanessa Perez-Ramos, Reg. No. 61,158, at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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